A Dedicated Setup for Test and Evaluation of Surface Mounted Power Switches

Manuel Fernández[1], Jaume Roig[2], Basil Vlachakis[2], Ignacio Castro[1], Diego González[1], Frederick Declercq[2] and Filip Bauwens[2]

[1] Universidad de Oviedo. Grupo de Sistemas Electrónicos de Alimentación (SEA)
Edificio Departamental nº 3. Campus Universitario de Viesques. 33204 Gijón. Spain
(e-mail: manuelfernandezingenieria@gmail.com)
[2] Power Technology Centre, Corporate R&D ON Semiconductor, Oudenaarde 9700, Belgium
(e-mail: jaume.roig@onsemi.com)

***Abstract*—This work reports the original design of a multi-purpose setup for characterization and benchmark study of power switches packaged on QFN (Quad Flat No-leads). More specifically, the setup evaluates advanced 650 V GaN and Silicon power switches by using a 300W/200kHz CCM boost converter. A genuine daughter board has been optimized by experiment and finite-element simulation to provide low thermal impedance, setup/package compatibility and to be easy-of-use. Moreover, the setup is equipped to automatically extract power losses, as well as, voltage and current waveforms for device model calibration.**

***Index Terms*—Superjunction, GaN, surface mounted, packaging, thermal management.**

I. INTRODUCTION

WITH the maturity of power semiconductor technologies, device specialization has been fostered for a wide portfolio of applications. In the market segment of high-frequency medium-voltage power electronics (> 100 kHz, 500 – 900 V), Silicon SuperJunction (SJ) technologies cope most of the market. Despite the Silicon supremacy, GaN-based switches are emerging as a more efficient solution. Even though their cost is still high, GaN-based switches are commercially available as stand-alone (E-mode) and cascoded (D-mode) GaN HEMTs [1]. From a historical perspective, power device manufacturers compared and ranked devices by means of simple Figures-of-Merit (FoMs) [2]. However, in a scenario where diverse technologies coexist for a given application, FoMs become inexact and meaningless. As a result, it is preferable to test device performance in the application itself. On the other hand, typical application test-boards are limited in terms of electrical/thermal operation conditions and device voltage/current sensing. Moreover, the power losses are normally measured in the whole application circuit, thus being complicated to identify particular contributions from their components. Ideally, a dedicated setup with similar conditions to the real application could be specially designed to cover all these needs. The aim of our work is to design, build and demonstrate a dedicated setup for test and evaluation of surface mounted devices addressed to 300W/200kHz PFCs with V_{OUT} = 400V. The setup demonstration is carried out by a comparative study between power switches, as well as, some validated tests of device characterization and simulation calibration.

II. SETUP DESIGN AND OPTIMIZATION

A. QFN Daughter Board

In a similar way that other common packages (TO-220, TO-247), 8x8 QFN (Quad Flat No-leads) has become a standard for surface mounted 650 V power switches [3,4]. This package can accommodate dies with an on-state resistance (R_{DSON}) not lower than 100 mΩ. The QFN version with an additional Kelvin contact significantly reduces the source inductance, thus enabling highly efficient high-frequency operation and overshoot minimization. On the other hand, the small size of the lead frame and the direct soldering to the board hamper the heat extraction and limit the maximum power loss. Another handicap of QFN packages is the complexity in replacing damaged parts from the main board, whereas TO-220, for instance, can be easily used as a plug-and-play package, QFN requires soldering in a reflow oven (considered option) or using a hot air station. In order to overcome the aforementioned issues, two adaptive daughter boards have been designed for different purposes.

A first daughter board, shown in Fig. 1a, is used to provide full compatibility to conventional equipment for TO-220 switch characterization. Similar to TO-220 package, a 3-pin allows GDS electrical connection to the board. Moreover, a series of thermal vias are drilled and metallized in a board area with the size of the QFN drain pad. Hence, after applying the solder paste, a low resistive electrical and thermal pad connects front to reverse sides of the daughter board.

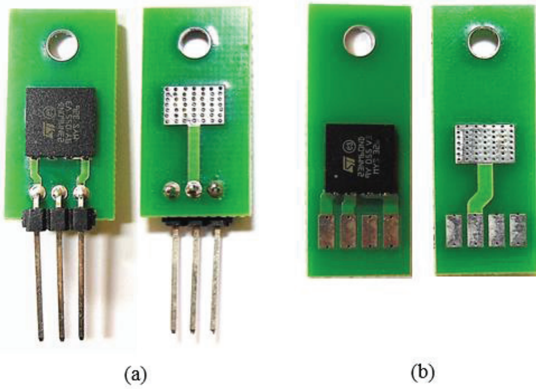


Fig. 1. Front and reverse sides of adaptive daughter boards for 8x8 QFN: (a) design TO-220-compatible with 3-pin connector, (b) design 4-pin edge connector.

In a preliminary study, the board design has been optimized by finite-element thermal simulations, using Autodesk CFD Simulation. In this sense, the number of thermal vias and the board thickness are selected to obtain the following trade-off between electrical and thermal characteristics:

- Series resistance: R_{DS} ~ 3 mΩ
- Parallel capacitances: C_{GD} and C_{DS} < 0.3 pF
- Thermal resistance: θ_{JA} ~ 13.5 °C/W (with heat sink)

An example of temperature distribution for one of the daughter boards attached to a heat sink (Aavid Thermalloy 530002B02500G) is shown in Fig. 2. In this specific case, a power dissipation of 4 W produces a maximum temperature of 76.4 °C inside the Silicon die.

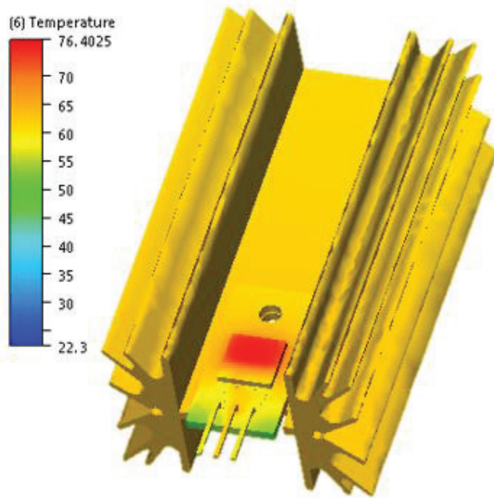


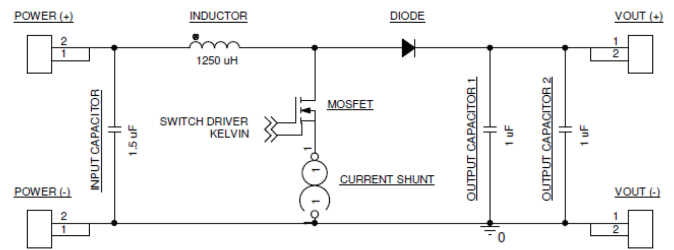
Fig. 2. Simulated temperature distribution in the adaptive daughter board on top of a heat sink (Aavid Thermalloy 530002B02500G). P_{OUT} = 4 W, steady state.

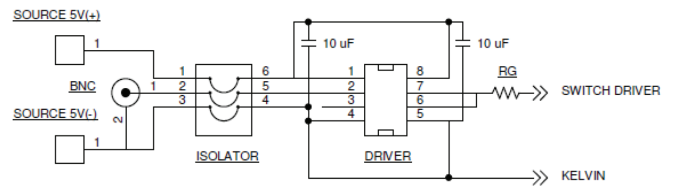
As the inner part of the device was partially modelled, the die can be defined as the power-dissipating component (4 W). A heat transfer coefficient for the whole heat sink describes convective heat transfer component (h = 2.8 W/m^2·K), with thermal boundary conditions set to natural convection. The variation of this parameter with temperature has been carefully calibrated by experimental analysis using an IR thermometer for measuring temperatures at different points while increasing the dissipated power. Once the thermal model is configured and the mesh is properly sized, the steady state solver is run.

A second daughter board, exhibited in Fig. 1b, has been designed for being used on a 4-pin edge connector. The thermal features are identical to the first design; however, the TO-220 large pin inductance is strongly reduced in our board. Furthermore, a Kelvin probe connects the die source electrode to the ground of the control loop. As a result, the source parasitic inductance is significantly reduced.

B. *Main Board*

A schematic of the main board is shown in Fig. 3a. The target design is a 100-to-400 V boost converter with 300 W output power. The boost converter is essentially constituted by a MOSFET switch, which is our device under test (DUT), a homemade inductor, a rectifying diode, three filtering capacitors and a fixed load. By using this topology, it is possible to keep the switching advantages of a double pulse tester without leaving the application field with inherent self-heating effects and a far less controlled environment.





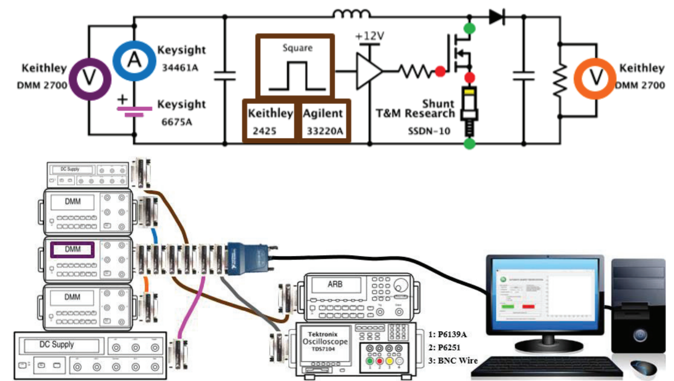


Fig. 3. Circuit diagram of the boost converter: (a) power loop, (b) control loop, (c) measurement scheme.

Since the purpose of this setup is to extract conclusions from the MOSFET device through efficiency measurements, a special care is taken on inductor and diode losses reduction. The homemade 1.25 mH low-loss inductor with ferrite core is designed by finding an optimum compromise between core and copper losses. A 600V SiC Schottky diode model C3D04060A from Cree is chosen for this design due to its switching characteristics with zero recovery current.

A picture of the manufactured board with all the components mounted is exhibited from top and bottom views in Figs. 5 and 6, respectively. Aside from DUT connector and driver, the board allocates MKP and MKT filtering capacitors. These capacitors are selected due to their superior dynamic performance and low equivalent series resistance. The metal tracks on the PCB board have been routed by using two metal layers. As a consequence, two major benefits are achieved. Firstly, the parasitic inductance in the power loop is diminished to less than 20 nH. A second advantage concerns the physical isolation of certain components, like the DUT, making them more accessible to measuring tools.

The bottom view of the main board contains two crucial elements of our circuit: the isolated driving interface and the coaxial shunt.

In order to protect the circuit from possible driving problems, an isolated driving interface is placed on the control loop for ground loop reduction. A schematic of this board is shown in Fig. 4.

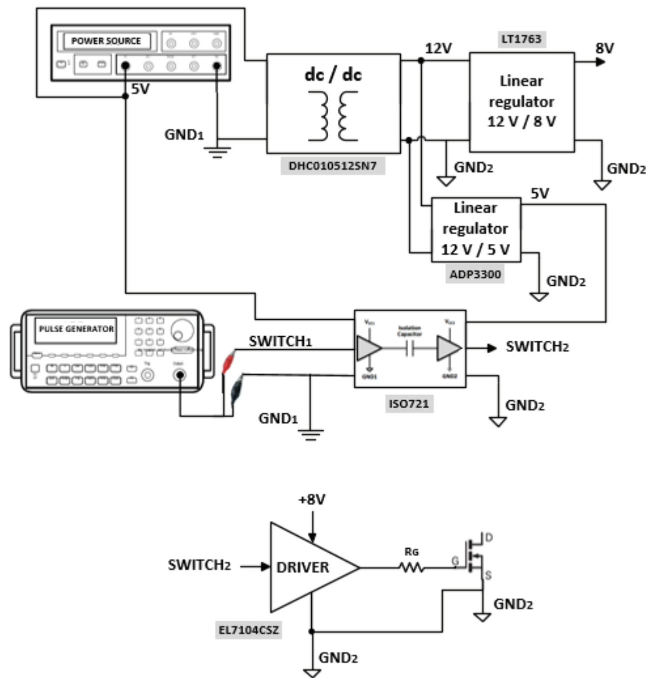


Fig. 4. Schematic of the isolated driving interface and the driver for normally-off devices.

A different objective has the coaxial shunt, which is used to sense the current flowing through the DUT. A SSDN-10, manufactured by T&M, is placed in series with the DUT source. The specifications of this shunt in Table I show accurate resistance, low parasitic inductance and high bandwidth.

Externally to the main board, a 536 Ω fixed load is made by using Welwyn and TE connectivity power resistors.

TABLE I. SPECIFICATIONS OF THE CURRENT SHUNT

Model	Resistance	Bandwidth	Risetime	E_{max}	Power
SSDN-10	0.1 Ω	2000 MHz	0.18 ns	2 J	2 W

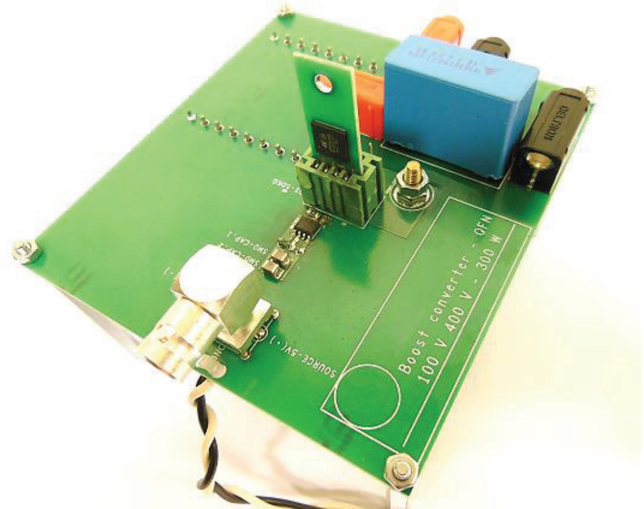


Fig. 5. Top view of the main board with the QFN adaptive daughter board inserted in the 4-pin edge connector.

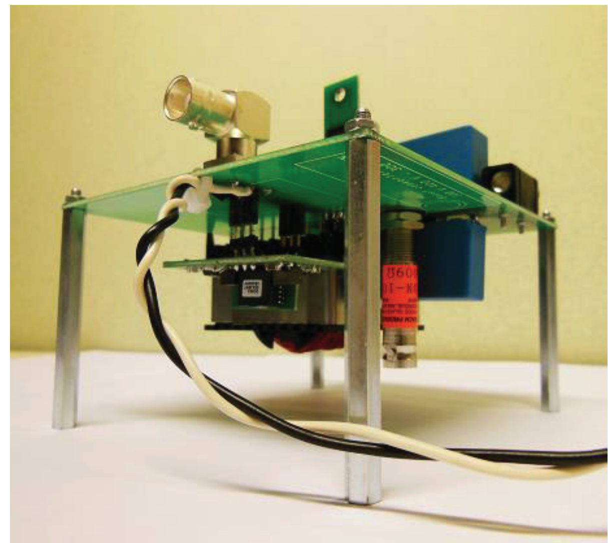


Fig. 6. Bottom view of the main board with the isolator daughter board and the coaxial shunt.

C. Automatic Extraction System

The acquisition of data related to efficiencies and waveforms has been fully automatized in our setup. In fact, a fully automated system was implemented by the use of software control techniques. This system has two main benefits. First of all, it ensures an appropriate level of both accuracy and repeatability. Secondly, it allows autonomous operation, as an error detection system would switch off the power supply in case of error.

The practical implementation of the automated system is done by GPIB connectors. These connectors were used for communication between computer and equipment, which is constituted by measurement system, power source and pulse generator. Among the most notorious instruments, calibrated digital multimeters from Keithley and Keysight, a Tektronix oscilloscope and both passive and differential voltage probes are used for measurement (P6139A and P6251 from Tektronix). Both measurement scheme and position of the probing points are indicated in Fig. 3c. In respect of computer side, Matlab and the Instrument Control Toolbox manage the connection, data acquisition, control and data processing. The control strategy is based on a PI controller and a closed voltage loop which consists on the connection of all the equipment. As the measurements are taken for a specific V_{OUT}/Power, the controller regulates the duty cycle until the output voltage is four times the input voltage for each power set by the user. Once the calibration of this parameter is fulfilled and the load has been cooled to ambient conditions, it starts the measurement stage at a speed of 25 efficiency measurements/s.

A graphical user interface is used for test configuration: DUT package selection, operating frequency, controller configuration and graphs visualization/extraction. Once configured, the software extracts the results for each power set, always on the same conditions, and exports them to an excel document after finishing every test. Many safety measures are taken to automatically detect wrong configurations and/or breakdown.

III. Experimental Results

A. Comparative analysis of efficiencies

This subsection is focused in the benchmarking study of different 650 V switches. All DUTs are listed in Table II, being possible to distinguish six Silicon SJ-FETs from one GaN switch. The latter is based on a co-packaged cascode topology. All these devices are commercially available, although the GaN switch implies a non-disclosure agreement to keep manufacturer and device model anonymous.

TABLE II. DEVICES UNDER TEST

Sample	Device	$R_{DS(ON)}$ [mΩ]	BV_{dss}[V]	V_{th}[V]
#1	CoolMOS CP [5]	180	600	3
#2	FDmesh II [6]	175	600	4
#3	SuperFET II [7]	170	600	3
#4	DTMOSIV [8]	160	600	3.2
#5	GaN switch	150	600	1.8
#6	DTMOSIV [9]	136	600	3.2
#7	MDmesh V [10]	135	650	4

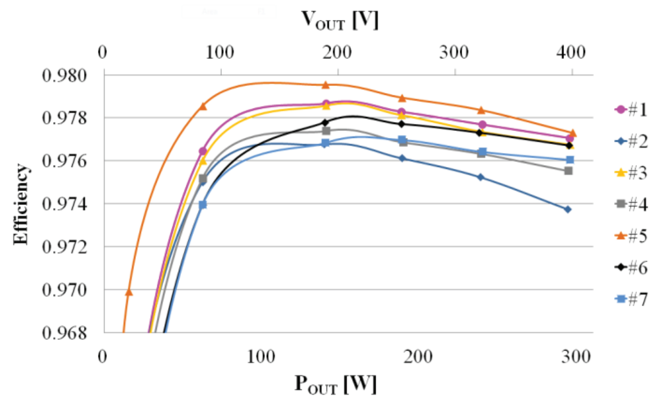


Fig. 7. Comparison of efficiency vs. P_{OUT} for devices listed on Table I. R_G = 6.8 Ω, V_{GS} = 12 V, f_{SW} = 100 kHz.

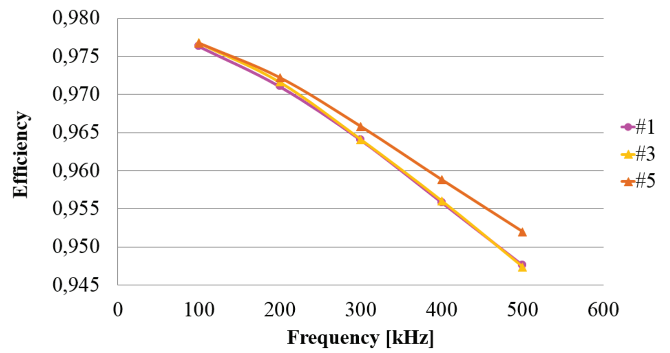


Fig. 8. Comparison of efficiency vs. f_{sw} for devices #1, #3 and #5. R_G = 6.8 Ω, V_{GS} = 12 V, V_{IN} = 100 V, V_{OUT} = 400 V, P_{OUT} = 300 W.

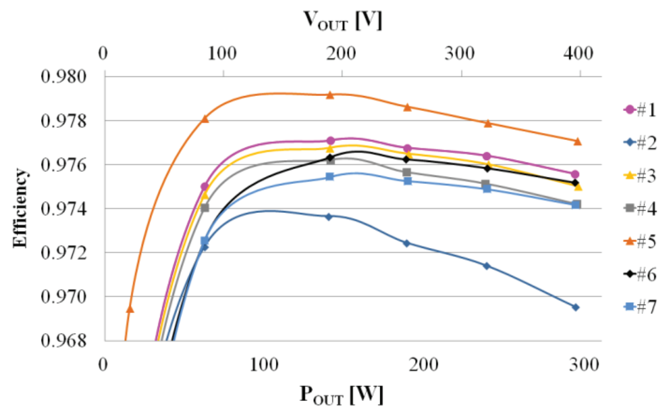


Fig. 9. Comparison of efficiency vs. Pout for devices listed on Table I. R_G = 15 Ω, V_{GS} = 12 V, f_{SW} = 100 kHz.

An efficiency comparison between all devices listed in Table II is shown in Fig. 7. In this case the boost converter is operated at f_{SW} = 100 kHz with R_G = 6.8 Ω and V_{DR} = 12 V. Under these conditions, it is remarkable that the GaN switch is not outperforming with respect to the best SJ-FETs. Nonetheless, it is observed from Fig. 8 that GaN shows its high potential at higher f_{sw}. As a matter of fact, the negligible difference on efficiency at 100 kHz becomes noticeable at 500 kHz. It can be inferred from Fig. 9 that the difference in efficiencies between GaN and SJ-FETs also becomes more evident by using larger R_G. More precisely, GaN efficiency

and waveforms are practically independent of R_G. Note that large R_G provides dV/dt control in Silicon technologies but not in a GaN cascode device.

Complementary to the efficiency measurements, DUTs on-state resistance (R_{ON}) is extracted for a wide current range by means of a FET-Tester. R_{ON} vs. I_D measurements, plotted in Fig. 10, were possible by using the TO-220 adaptive daughter board. Eventually, R_{ON} will help in calculating conduction power losses.

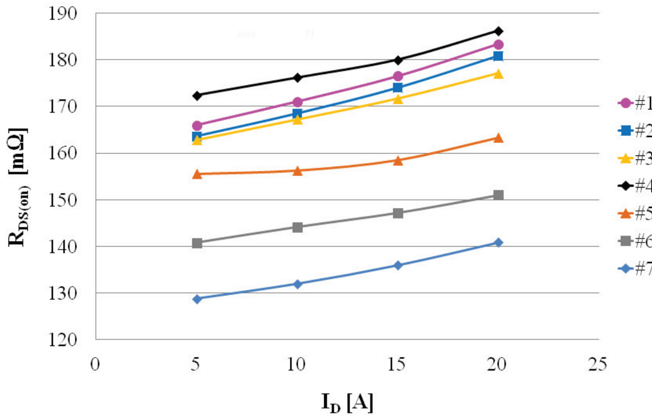


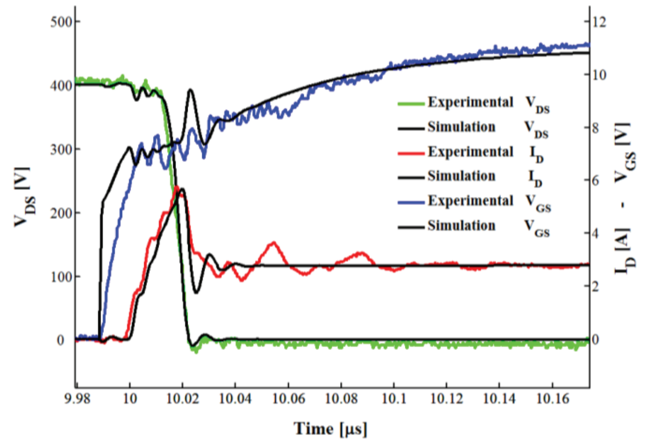
Fig. 10. Comparison between on-state resistance vs current for devices listed on Table I. Measurements extracted with FET-Tester (FETtest 3600E).

B. *Device characterization.*

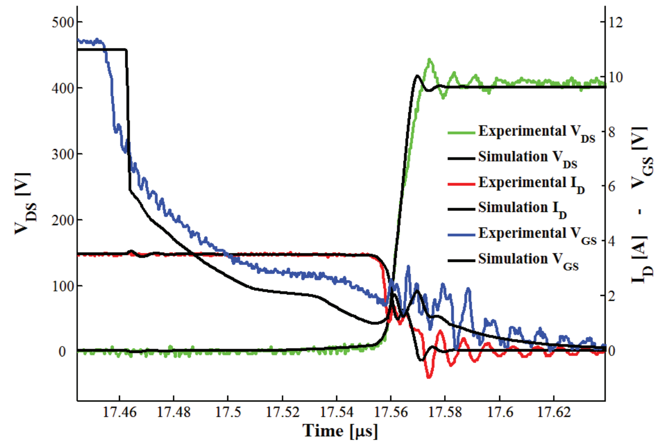
Another relevant use of our multi-purpose board is the device characterization of some of the transition charges, like Q_G, Q_{GD} and Q_{GS}. This test implies sensing of the current sourcing and sinking into the DUT gate while a constant gate-source voltage is applied, and is preferably performed using a large R_G (150 Ω). During these tests the boost converter is operated at f_{SW} = 100 kHz with V_{GS} = 12 V and V_{IN} = 40 V which results in V_{DS} = 160 V and I_D = 1.25 A. The results are almost the same for higher voltages (V_{DS} = 400 V), so it is preferred to lower the power losses and prevent the device from breaking because of using a larger gate resistance. The test results compared to information provided in the datasheet by vendors is summarized in Table III. In the overall, a good match is obtained with difference below 5 %, although some specific devices show larger discrepancies (> 13 %).

TABLE III. EXPERIMENTAL SWITCHING CHARACTERISTICS

Sample	Q_G[nC] Datasheet	Q_G [nC]	Q_{GD} [nC]	Q_{GS} [nC]
#1	32	36.17	9.93	7.25
#2	69	67.20	32.23	10.42
#3	57	54.59	17.19	10.42
#4	38	34.48	10.23	7.85
#5	6.2	5.73	2.29	2.20
#6	48	46.47	13.42	9.76
#7	45	42.04	14.36	10.91



(a)



(b)

Fig. 11. Comparison between measured and simulated transient waveforms in a prototype of a SJ technology for (a) turn-on and (b) turn-off. R_G = 6.8 Ω, V_{GS} = 12 V, V_{IN} = 100 V, V_{OUT} = 400 V, P_{OUT} = 300 W.

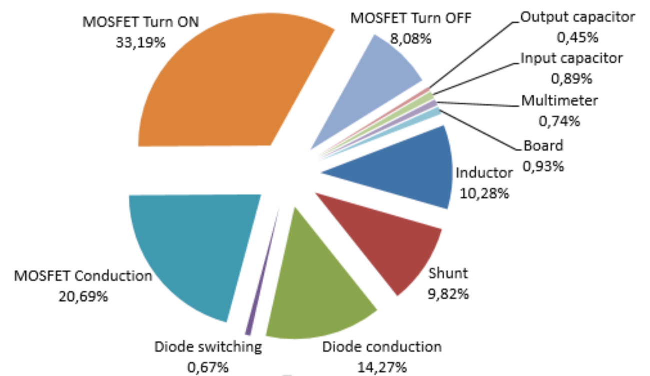


Fig. 12. Power loss breakdown for a prototype of a SJ technology. V_{IN} = 100 V, V_{OUT} = 400 V, R_G = 6.8 Ω, f_{SW} = 100 kHz.

C. Calibration of simulations and power loss analysis

The setup has also been used for calibration of mixed-mode simulations carried out with Sentaurus™ [11]. Being an interdisciplinary approach, mixed-mode combines finite-element with SPICE simulations. For such a calibration, a high degree of accuracy is required in sensing the DUT source current (equal to the drain current). The device selected for this calibration is a prototype of a SJ technology under development. This selection is based on the complete knowledge of the fabrication process for calibration of device physical models. In fact, process simulation with Sentaurus Process is used as preliminary step to obtain SJ-FET finite-element structure. Afterwards, the electrodes of such structure are linked to the corresponding nodes of the boost converter SPICE circuit, which includes all parasitic inductances and resistances originated by package and board. Eventually, once the whole system is defined, physical (Poisson and electron/hole current continuation) and circuit equations are consistently solved by using iterative methods. The comparison between simulation and experimental curves in Figs. 11a and 11b proves that the physical models are precise in the description of the device electrical characteristics.

Combining simulation and measurement information, a deep analysis of the different power loss contributions is possible. As a matter of example, Fig. 12 exhibits the power loss breakdown for our specific DUT. The identification of the source for the different power losses is a powerful knowledge to further optimize power switches and, finally, system performance.

IV. Conclusion

A comprehensive analysis of 650 V QFN-packaged switches is presented in this paper by means of a dedicated setup. In a benchmarking study, the most advanced technologies have been ranked in accordance to their electrical performance, being GaN technology superior to Silicon SJ-FETs at high frequency and high R_G. Furthermore, the use of the setup for characterization and calibration of simulations has been also demonstrated for an own SJ-FET prototype.

References

[1] S. Levin, "Vendor Positions in the High Voltage GaN Commercialization Race", Bodo's Power Systems, Feb. 2013, pp. 34-36.

[2] A. Q. Huang, "New Unipolar Switching Power Device Figures of Merit," *IEEE Trans. Electron Devices*, vol. 25, pp. 298–301, May 2004.

[3] Infineon technologies Ag. - Q&A ThinPAK 8x8 - New leadless SMD package for CoolMOS, May 2010. V 1.1

[4] W. Choi, D. Son, D. Kim, "Advantages of Low Parasitic Inductance Packages of Power MOSFET for Server Power Applications," in *Proc. International Power Electronics Conference*, 2014, pp. 2914–19.

[5] Infineon, "CoolMOS™ CP 600V Power Transistor", IPL60R199CP datasheet, Jan. 2012 [Rev. 2.2].

[6] STMicroelectronics, "FDmesh™ II Power MOSFET (with fast diode) in PowerFLAT™ 8x8 HV package", STL23NM60ND datasheet, Apr. 2010 [Revised Mar. 2013].

[7] Toshiba, "MOSFETs Silicon N-Channel MOS (DTMOSIV)", TK16V60W datasheet, May 2013 [Revised Feb. 2014].

[8] Fairchild, "N-Channel SuperFET® II MOSFET" FCMT199N60 datasheet, Aug. 2014 [Rev. C2].

[9] Toshiba, "MOSFETs Silicon N-Channel MOS (DTMOSIV)", TK20V60W datasheet, Mar. 2013 [Revised Feb. 2014].

[10] STMicroelectronics, "MDmesh™ V Power MOSFET in a PowerFLAT™ 8x8 HV package", STL31N65M5 datasheet, Oct. 2013 [Rev. 1].

[11] Sentaurus TCAD Tools Suite. Synopsys 2010.